UNIVERSIDAD DE ALCALÁ ESCUELA POLITÉCNICA SUPERIOR DEPARTAMENTO DE ELECTRÓNICA		GRADO EN INGENIERÍA EN ELECTRÓNICA Y AUTOMÁTICA INDUSTRIAL	
ASIGNATURA	SISTEMAS ELECTRÓNICOS DIGITALES	CURSO	2015-2016
APELLIDOS		DNI	
NOMBRE	SOLUCIÓN	GRUPO	

ENTREGABLE TEMA 4

Conexión de memorias SDRAM y DUAL-PORT al EMC

a) A partir del esquema de la tarjeta de desarrollo **LPC-LNX-EVB** basada en el LPC1788 (disponible en Documentación adicional del Tema 3) :

   a. Indique la capacidad y organización de la memoria SDRAM, así como el rango de direccionamiento dentro del mapa.

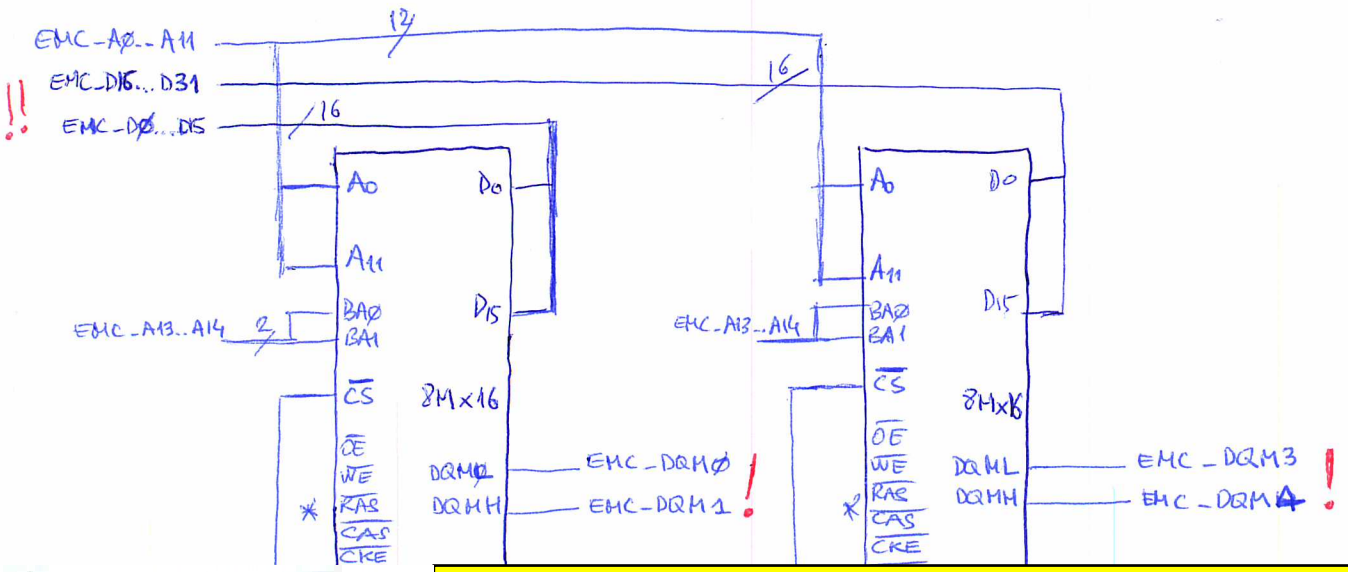
IS42S32800D → 2M x 32bits x 4 bancos → 8M x 32 → 256 Mbits

EMC_DYCS0 → 0xA000.0000 – 0xA1FF.FFFF

   b. Proponga una solución para reemplazar el chip de SDRAM e implementar la misma capacidad utilizando chips MT48LC8M16A2.

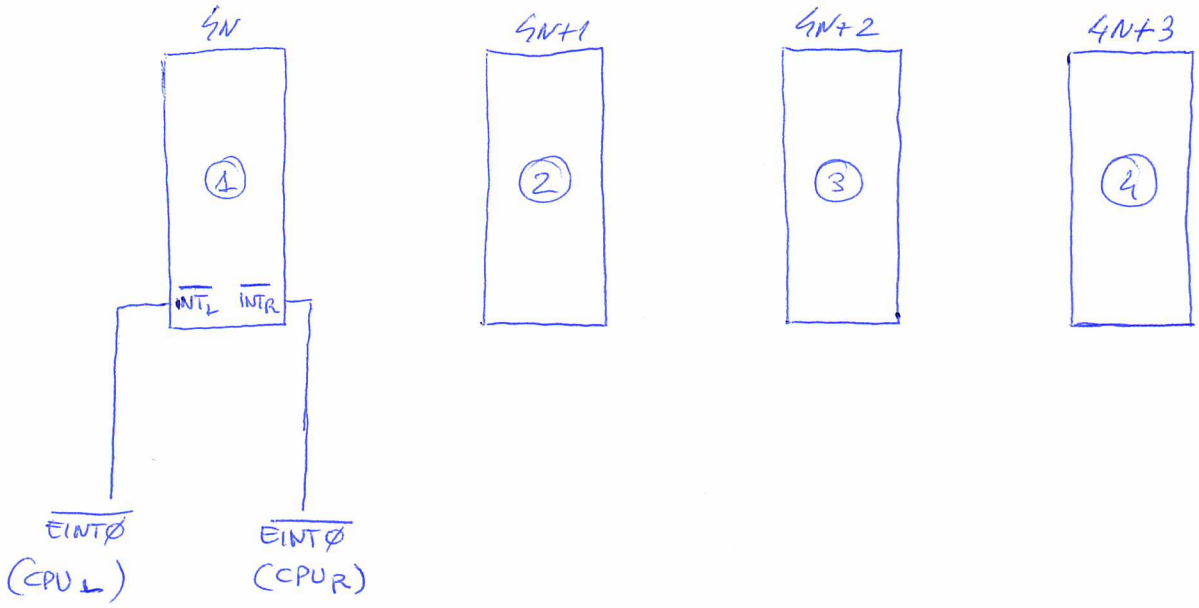
MT48LC8M16A2 → 8M x 16 → 2M x 16 bits x 4 bancos (ver diagrama)

Se necesitan 2 chips.



b) Se desea añadir 128Kbytes de memoria Dual-Port a partir del chip CY7C007 para poder compartir esta memoria con un segundo LPC1788 en modo 32 bits. Como mecanismo de arbitración se elige el de interrupción.

A partir de la solución del apartado b) del entregable del curso 2014-1015, indique las nuevas direcciones empleadas para la arbitración si en lugar de utilizar el chip 4 se utilizase el chip 1, y cómo quedaría afectado el proceso de arbitración.



DIR. arbitración CPU_L
- Øx9ØØ1.FFFC (última chip 1)
- Øx9ØØ1.FFF8 (penúltima chip 1)

2M×32×4bancos ≡ 8M×32 !!

U6 — IS42S32800D

U4 — M29W128GL70N6E

RN2 — EXB28V220JX

RN1 — EXB28V333JX

EmCraft CONFIDENTIAL

Emcraft Systems			
External Flash, SDRAM, and Reset			
Size A3	FCSM No.	DWG No. LPC-LNX-EVB	Rev 1.0
Scale	2012-01-18	Sheet 3 of 6	

DEVICE OVERVIEW

The 256Mb SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 3.3V V_{DD} and 3.3V V_{DDQ} memory systems containing 268,435,456 bits. Internally configured as a quad-bank DRAM with a synchronous interface. Each 67,108,864-bit bank is organized as 4,096 rows by 512 columns by 32 bits.

The 256Mb SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK. All inputs and outputs are LVTTL compatible.

The 256Mb SDRAM has the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during burst access.

A self-timed row precharge initiated at the end of the burst sequence is available with the AUTO PRECHARGE function enabled. Precharge one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

SDRAM read and write accesses are burst oriented starting at a selected location and continuing for a programmed number of locations in a programmed sequence. The registration of an ACTIVE command begins accesses, followed by a READ or WRITE command. The ACTIVE command in conjunction with address bits registered are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The READ or WRITE commands in conjunction with address bits registered are used to select the starting column location for the burst access.

Programmable READ or WRITE burst lengths consist of 1, 2, 4 and 8 locations or full page, with a burst terminate option.

FUNCTIONAL BLOCK DIAGRAM (FOR 2Mx32x4 BANKS)

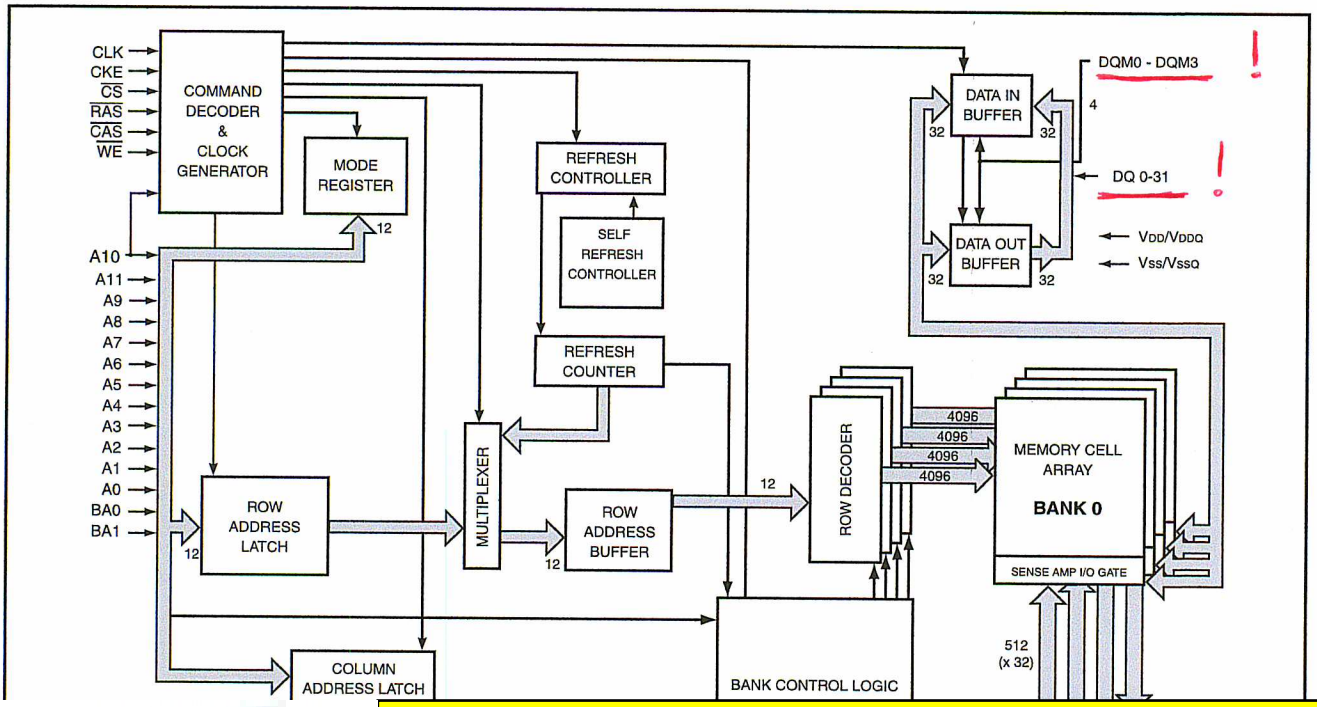


Figure 3: 8 Meg x 16 Functional Block Diagram